What is claimed is:

1. A semiconductor device of a double diffused MOS structure employing a silicon carbide semiconductor substrate, the device comprising:

a silicon carbide semiconductor epitaxial layer provided on a surface of the silicon carbide semiconductor substrate and having a first conductivity which is the same conductivity as the silicon carbide semiconductor substrate; and

an impurity region formed by doping a surface portion of the silicon carbide semiconductor epitaxial layer with an impurity of a second conductivity, the impurity region having a profile such that a near surface thereof has a relatively low second-conductivity impurity concentration and a deep portion thereof has a relatively high second-conductivity impurity concentration.

2. A semiconductor device as set forth in claim 1, wherein a second-conductivity impurity concentration in an outermost surface portion of the impurity region is controlled to be lower than a first-conductivity impurity concentration in the silicon carbide semiconductor epitaxial layer.

3. A semiconductor device manufacturing method for manufactureing a semiconductor device of a double diffused MOS structure employing a silicon carbide semiconductor

substrate, the method comprising steps of:

forming a silicon carbide semiconductor epitaxial layer having a first conductivity on a surface of the silicon carbide semiconductor substrate, the first conductivity being the same conductivity as the silicon carbide semiconductor substrate; and

doping a surface portion of the silicon carbide semiconductor epitaxial layer with an impurity of a second conductivity to form an impurity region having a profile such that a near surface thereof has a relatively low second-conductivity impurity concentration and a deep portion thereof has a relatively high second-conductivity impurity concentration.

4. A semiconductor device manufacturing method as set forth in claim 3, wherein the surface portion of the silicon carbide semiconductor epitaxial layer is doped with the impurity of the second conductivity by single-step ion implantation in the impurity region forming step.

5. A semiconductor device manufacturing method as set forth in claim 3, wherein the impurity region is formed as having a profile such that a second-conductivity impurity concentration in an outermost surface portion thereof is lower than a first-conductivity impurity concentration in the silicon carbide semiconductor epitaxial layer in the impurity region forming step.